ABSTRACT

A test pattern generation circuit ~~(100)~~ outputs a test pattern ~~(TP)~~ during a clock phase adjustment period. A flip-flop circuit ~~(110)~~ latches the test pattern ~~(TP)~~ at the fall of a shift clock ~~(SCK)~~ and outputs it as a test pattern ~~(Tpa)~~. A latch miss detection circuit ~~(130)~~ outputs a latch miss detection signal ~~(LM)~~ indicating presence/absence of a latch miss generation according to the test pattern ~~(TPa)~~ and a delay shift clock ~~(DSCK)~~. A clock phase controller ~~control section (120)~~ delays the shift clock ~~(SCK)~~ according to the latch miss detection signal ~~(LM)~~, thereby outputting a delay shift clock ~~(DSCK)~~.